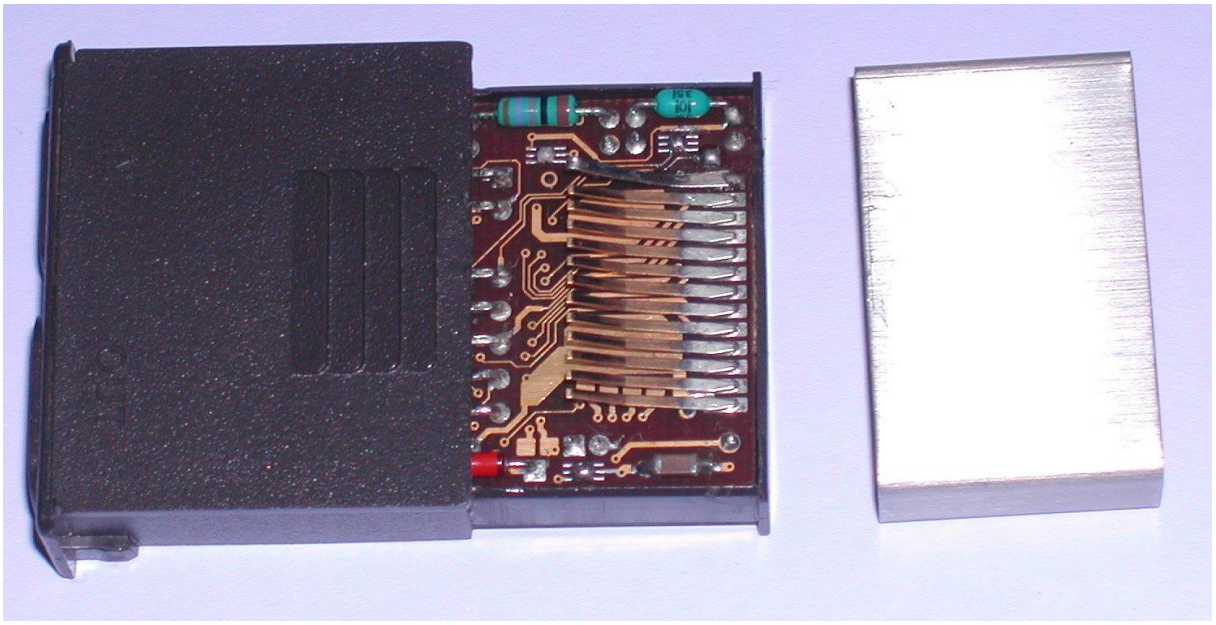
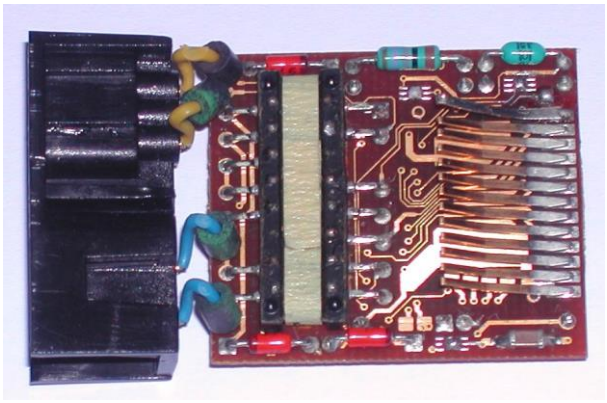
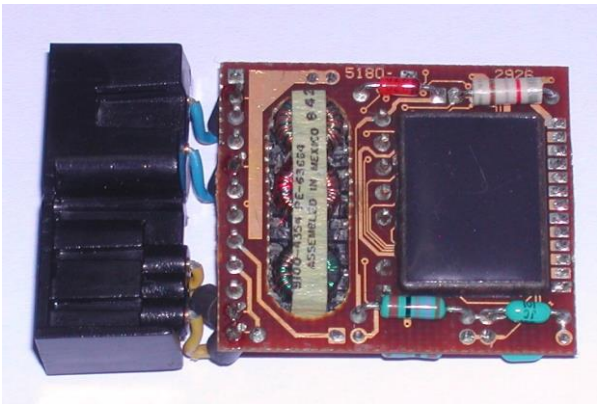
HP-IL module 1A investigation
(HP-71B)

J-F Garnier, Nov 2009



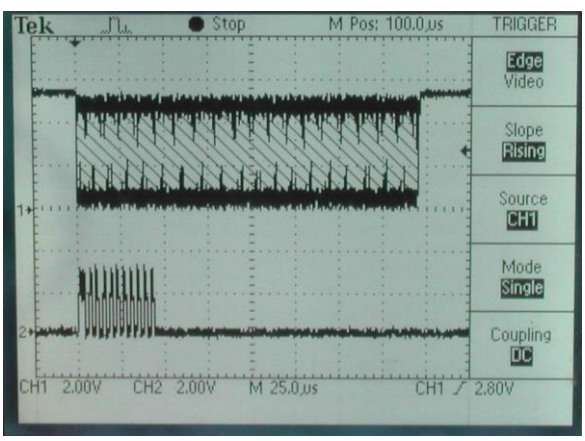


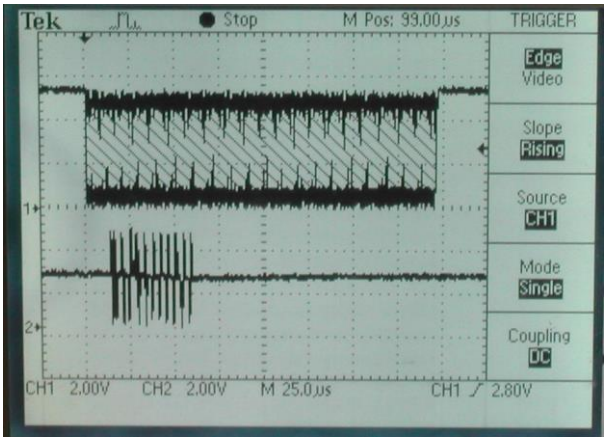


Identified components:
4 Zener diodes,
2 resistors 178 Ohms,
2 capacitors,
1 inductor 270 uH,
1 SMD decoupling capacitor (connected between Vcc and Vss),
HP-IL pulse transformer.

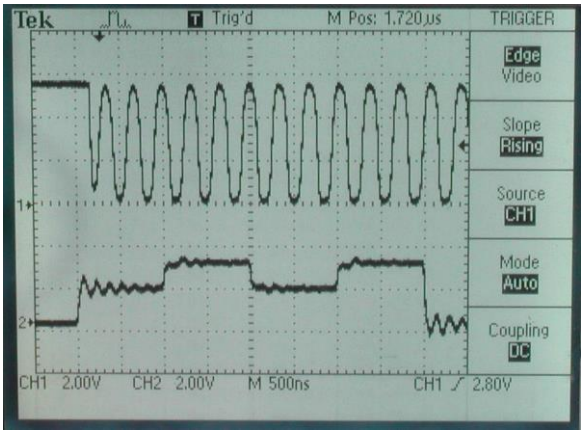
Current consumption at 5.5V:
idle 0.6uA
operating as a device (PLIST from an external HP71B): 1.7 uA average

The HPIL module hardware is completly static in idle state, the clock required for the frame processing is running only when needed, it is stopped when there is no HPIL activity and is started at the begining of the incoming frame:



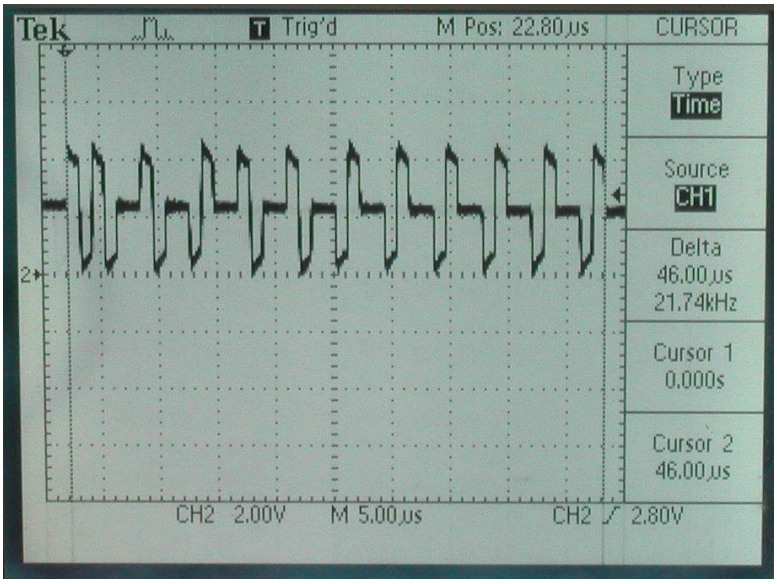


Trace 1 is the clock of the HPIL module (signal picked on the inductor),
trace 2 is the HPIL signal (left: incoming frame, right: transmitted frame).

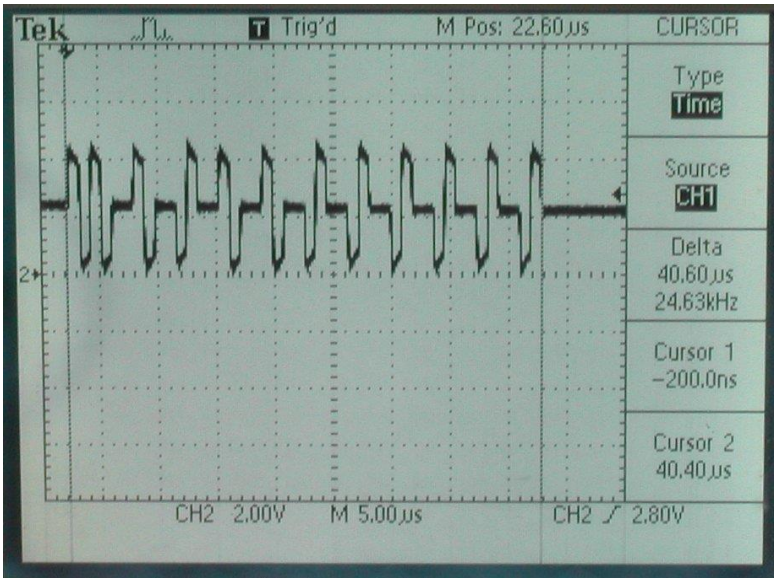


Detail of the clock startup: the clock is stable 500 ns after the beginning of the incoming frame.

Measured frequency with scope probe: 2.9 MHz.



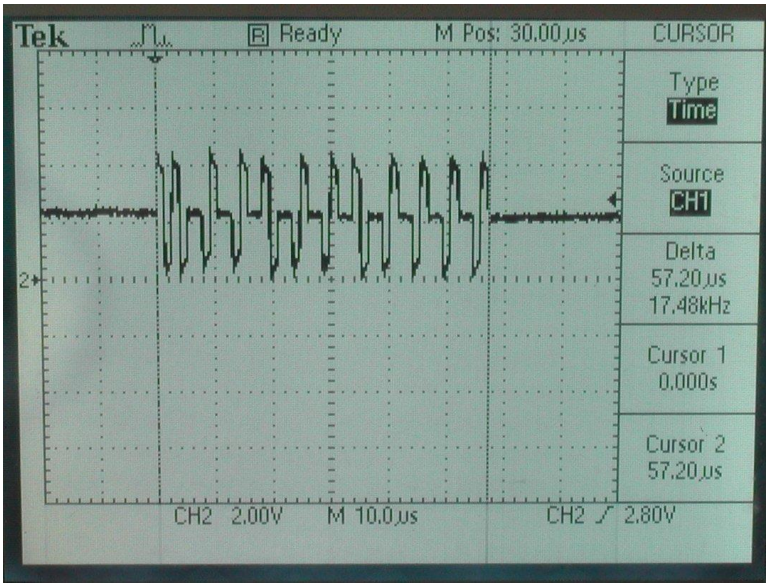
Transmitted HPIL frame with scope probe still attached on clock: duration= 46 us.
A frame is 11 * 4 = 44 cycles
Measured frequency with scope probe: 2.9 MHz
There is 46us/44 / (1/2.9MHz) = 3 clock periods per cycle



Transmitted HPIL frame with scope probe removed from clock: duration= **40 us**.

The nominal frame duration is specified as 11 * 4 us = **44 us +/- 5%.**

This is the issue of some the module version 1A: HPIL timings are not accurate and are some modules are out of spec (10% deviation here).



Attempt to correct the clock by adding a 10 pF capacitor in // with the inductor:
Frame duration is now 57us.
This does not work.