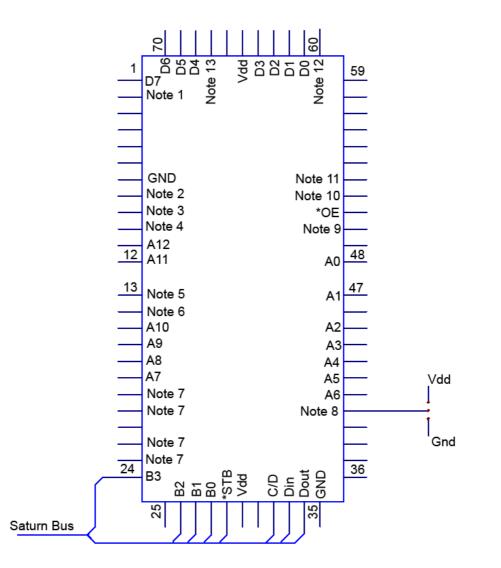
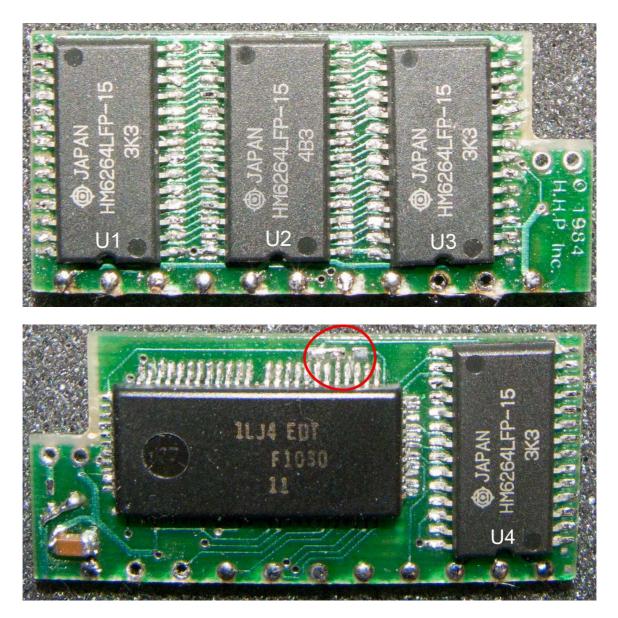
The following pinout of the HP 1LJ4 chip, used to interface industry standard memory to the Saturn bus as found in the HP-71B, is based on my observations of HHP card reader port memory modules. For the purposes of this document I will use the term "module" to refer to the individual sub assemblies HHP used in various combinations to build card reader port memory expansions. I have had access to 3 different flavours of modules, 32K RAM composed of four 8K SRAMs, 32K RAM composed of a single 32K SRAM and a 32K EPROM module. Information about the pin that controls the last chip in module bit returned when the device is polled is courtesy of J.F. Garnier. In the notes below I will refer to the RAM module with four 8K SRAMs as RAM1, the RAM module with a single 32K SRAM as RAM2, and the EPROM module as ROM.



Note 1: On RAM1 this pin is tied to ground on RAM2 and ROM this pin is tied to Vdd. It would appear this is one of the pins that determines the memory device configuration.

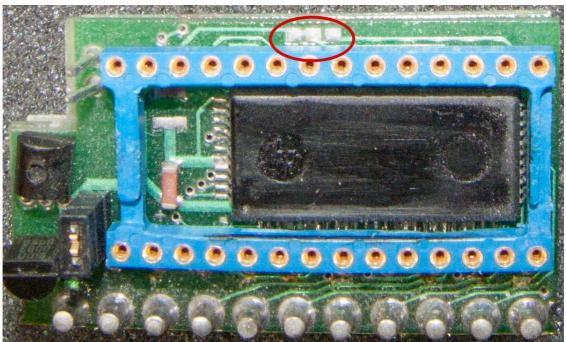
- Note 2: On RAM1 this is CS on U1, On RAM2 this is CS and on ROM it is not connected.
- Note 3: On RAM1 this is CS on U4, On RAM2 and ROM this is A14
- Note 4: On RAM1 this is CS on U2, On RAM2 and ROM this is A13
- Note 5: On RAM1 and RAM2 this pin is tied to GND on ROM it is tied to Vdd This pin would appear to determine if the module reports as RAM or ROM.
- Note 6: On RAM1 this pin is tied to Vdd on RAM2 and ROM it is tied to GND this appears to be another pin that determines the memory device configuration.
- Note 7: On the RAM 1 module there appears to be connections to these pins however they are not connected on the RAM2 or ROM modules which would suggest that they are pins with no internal connection that where just used as a convenient place to route signals.
- Note 8: The state of this pin determines weather the module reports as the last chip in the module or not. When it is tied high it reports as the last chip in module but when it is low it does not and its capacity will get added on to the next memory device in his way logical memory blocks larger than 32K can be created.
- Note 9: On RAM1 this is CS for U3, this pin is not used by RAM2 or ROM.
- Note 10: On RAM1 and RAM2 this is the WE pin, it is not used on ROM.
- Note 11: This pin is used for CS on the ROM it is not used on RAM1 or RAM2
- Note 12: On RAM1 this pin is tied to Vdd on RAM2 and ROM it is tied to GND this appears to be another pin that determines the memory device configuration
- Note 13: On RAM1 this pin is tied to Vdd on RAM2 and ROM it is tied to GND this appears to be another pin that determines the memory device configuration



Front and back side of the four 8K SRAM module, Note chip number arbitrarily assigned relate to notes above. The red circle shows the location of the last chip in module jumper, as show it is tied high for last chip.



RAM module with single 32K SRAM. The other side of this module is identical allowing for 64K on the one module. The red circle shows the location of the last chip in module jumper and in this case it is tied to ground and the other side is tied high so this reports as a 64K module. By default J01 is connected and has to be cut before jumpering J2.



ROM module with the EPROM removed. The transistors on the left control power to the EPROM, and only turn it on when it is being accessed, this was likely done to save batteries especially if a NMOS EPROM was installed. There are jumpers on the the module to accommodate smaller capacity EPROMs, however it will always report 32K of ROM and when smaller than 32K EPROMs are used they will appear more than once in the 32K space. One thing that has been observed is the modules with four 8K SRAMs may be more prone to failure. I have had two modules in one assembly that had bad SRAMs and I know of other people that have also encounter failed SRAMs. One of the things that may contribute to this is most 8K SRAMs that I have seen the specifications for are rated for a maximum Vcc of 5.5V and in a 71B the positive voltage is close to 6V or nearly 10% over the rated voltage. After swapping a couple chips on a module and still finding it was failing, I removed all of the 8K chips and replaced it with a single 32K SRAM. The 32K SRAMs have the advantage that they are normally rated for a maximum Vcc of 7V so may be more robust.

Both the 8K and 32K SRAMs are 28 pin parts and there are actually only 2 pins different between them making the swap relatively easy. On the 8K part pin 1 is not connected and on the 32K part it is A14. On the 8K part pin 26 is a second active high chip select pin, on the 32K part this is A13.

Please refer to the pictures of the four 8K SRAM module above and the steps below to make the modification. I chose to install my 32K chip in the U1 position as it has pin 20 (CS) connected to the right pin on the interface chip. This position will have the least number of alterations.

- 1. Remove all of the 8K SRAMs.
- 2. You will need to make a couple of cuts on the pads in the U1 position. On the 8K SRAM pin 1 is not connected so when the board was laid out the plus voltage line was run right through pins 1 and 28 on all three chips, you will need to isolate pin 1. On the 8K chips pin 26 is tied high so this pin will need to be isolated as well.
- 3. After isolating pins 1 and 26 mount the replacement 32K SRAM.
- 4. Connect pin 1 to the pad for pin 20 in the U4 position this will connect it to pin 9 of the interface chip.
- 5. Connect pin 26 to the pad for pin 20 in the U2 position this will connect pin 26 to pin 10 of the interface chip.
- 6. Now you need to make some connection changes on the interface chip, I found it easiest to lift the pins and make the connections in the air. Pin 2 is connected to GND it needs to be connected to Vdd. Pin 14 is connected to Vdd it needs to be connected to ground. Pin 60 is connected to Vdd it needs to be connected to GND. Pin 67 is connected to Vdd it needs to be connected to GND.

You should now have a working 32K RAM module with a single 32K SRAM in place of the four 8K SRAMs.

Paul Berger April 7, 2018