Siliconix

A SYSTEM SOLUTION TO HP-IL EQUIPMENT INTERFACE

Robert J. Zavrel Jr.
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INTRODUCTION

Siliconix manufactures several high performance components which lend themselves nicely to portable equipment. For a 4-½ digit HP-IL compatible DVM, Siliconix now offers a "systems solution" to the designer of such a device. With the exception of a few standard 4000 series CMOS ICs, all the special integrated circuits are offered by Siliconix. The DVM is based on the Si7135, a high-quality, single chip, dual-slope integrating A/D converter. The circuit used to interface the Si7135 to the HP-IL contains 23 standard 4000 series CMOS ICs. This hardware interface solution will be simplified to a 28 pin DIP interface IC. This IC allows direct connection to the Hewlett-Packard HP-IL standard "GPIO". Additionally, Siliconix offers three devices which complete the specialized DVM IC requirement. The DF412 provides a local LCD driver which will allow the DVM to operate as a stand-alone device. Two SD5002 analog switches are arranged to provide an analog input multiplexer which boasts over 100 db. channel-to-channel isolation. Finally, an Si7661 voltage converter eliminates the need for a negative power supply, thus a single 5 volt supply is all that is necessary.

The HP-IL "interface loop" is a data communications system designed as a portable, low cost, and high quality instrument controller. It is quite suitable for lab environments where easy programming is desirable. The powerful and popular HP-41 handheld computer or the HP-75C portable computer can be used as controllers for up to 31 "HP-IL devices" in the loop. Hewlett-Packard manufactures a wide variety of HP-IL compatible devices including a printer, timer, video interface, and DVM (Reference 1). For convenience the HP-41 will be used as the controller in this paper. A detailed description of HP-IL is beyond the scope of the paper, but a basic understanding of HP-IL is necessary to render this interface technique meaningful.

HP-IL INTERFACE CIRCUIT/INTERFACE IC HANDSHAKING

Care must be taken to avoid confusion of terms. The HP-IL interface circuit contains two basic ICs. It is this circuit which takes the serial IL pulses and routes the data to the two-way data bus, the appropriate handshake and other control pins. Taken together this assemblage of data and control pins is called "GPIO" or "general purpose input/-output". Hewlett-Packard offers four approaches to realizing the HP-IL interface circuit. Details of these approaches are available from Hewlett-Packard. The "Interface IC" interfaces the Si-7135 digital outputs to the GPIO bus. (Figure 1).

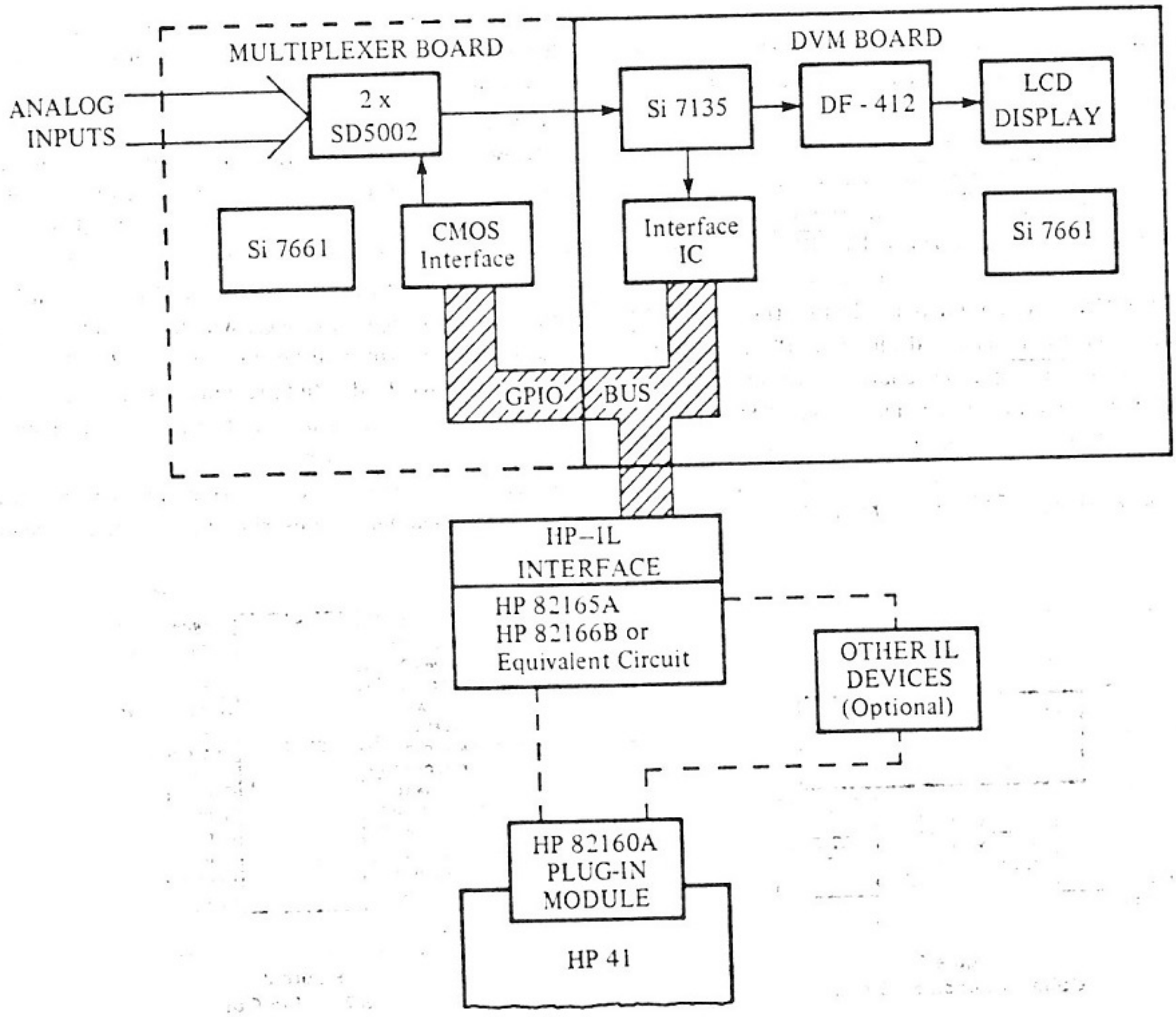

Figure 1
HP-IL Multiplexer/DVM System

Contained within the HP-IL interface circuit are the 28 pin DIP ILB3-0003 from Hewlett-Packard and the Mostek 1820-2810 40 pin single chip microcomputer. The ILB3-0003 contains multiple registers and extensive circuitry for the HP-IL interface. The microcomputer acts as an HP-IL device controller and provides the GPIO data and control pins later to be discussed in detail. This Mostek microcomputer is made with a special mask for HP-IL and must be purchased from Hewlett-Packard. These ICs are arranged around two 8-bit data busses labeled as DA and DB. In the DVM and multiplexer circuits, the DB bus is used only for data transfers between the 1820-2810 and the ILB3-0003. The DA is used as the bi-directional bus between the 1820-2810 and the DVM. Because ASCII characters are seven-bit words, the eighth bit of the eight-bit bus should be held low when ASCII is being transmitted. The circuits described here link the GPIO standard interface to the specialized data and control pins of the Si7135 4 ½ digit DVM chip and a multiplexer. The multiplexer circuit is also relatively simple, needing only a few standard CMOS ICs.

ASCII characters are used for all data transfer in HP-IL. Data transfer can flow to an external device such as a printer or from an external device such as a DVM. Two device modes are consequently defined as listener and talker. Data transfer between an HP-IL station and its corresponding peripheral device can utilize six "handshake" and additional command pins located on GPIO. Three handshake pins are used for the listener mode, and three are used for the talker mode. The two handshake modes are very similar. When listener is ready to accept data, a "Ready" pin is taken low (logic true). The talker may respond at this point if it has data to send with an ASCII character on the data bus and a low "Data Valid" pin. Finally, if the listener receives the data, it sets the "Data Confirmed" pin low completing the handshake sequence.

Several levels of handshaking are possible using the three handshake pins in different combinations. For the Siliconix DVM, the talker handshaking is very simple. "Data confimed" is not used, and the "Ready" and "Data Valid" pins are hardwired together. "Ready" and "Data Valid" correspond to the $\overline{\text{RDYO}}$ and $\overline{\text{DAVI}}$ pins for the talker handshake. In addition, the $\overline{\text{GETO}}$ pin is used to intialize a reading which is fed to the controller. The $\overline{\text{GETO}}$ pin is set low by a "TRIGGER" command in the computer software program. The "IND" command is used after the "TRIGGER" command to actually read in decimal data from the HP-IL device. The low $\overline{\text{GETO}}$ pin sets a latch in the interface IC in turn allowing a counter to sequence seven ASCII characters to the HP-IL. The counter is sequenced as the $\overline{\text{RDYO}}$ pin is set low if three conditions are met. Sequencing is prevented during the $\overline{\text{GETO}}$ pulse by the first of three conditional "AND" gates controlling the counter. The second gate is activated by the "TRIGGER" latch. In addition, an optional third gate is provided by the interface IC's ENABLE pin to be discussed later.

The seven ASCII characters provide for a polarity character, five digits, and a hardwired ASCII "LF" command. This character is recognized by the controller as an "End of Data" statement. The counter is allowed to sequence one more step after the "LF" command which resets itself and the "TRIGGER" latch. The read cycle is now complete, and the interface IC is ready to send another reading. A very simple seven line program in the HP-41 will initialize the DVM, read in the data, display the data, and loop back to take another reading. This program is shown in Table 1.

Figure 1 shows a functional block diagram of the system that contains several levels of asynchronism. The HP-41 is asynchronous to HP-IL; HP-IL is asynchronous to the interface IC; and the interface IC is asynchronous to the Si7135. The interface IC must account for random events at all three levels and convert the polarity and strobed BCD outputs to the proper ASCII characters. A subtle but desirable trait of the interface is that it should not allow a reading by the HP-IL while the Si7135 is latching in new data. Additionally, the interface should not allow the latching of data while the HP-IL is reading. Either condition would result in an invalid entry. The ENABLE pin when used with the circuit in Figure 2 will prevent the counter from sequencing the ASCII characters. The result will be a repetition of a single character which will fill the HP-41 X Register. In turn, this may be checked with HP-41 software, and the data will be deleted preventing an HP-IL read during a latch change. Alternatively, this gate may be held high if an occasional invalid reading is permissible. With this configuration, about 3% of the readings will be invaild. "Invalid" is used here to describe the condition of reading in the five digit number from two separate Si7135 writings. For example, if the Si7135 latches in new data to the interface IC while the HP-IL is reading, perhaps the first two digits may be from the old voltage reading while three would be from new data. The other invalid condition is prevented by stopping the Si7135 with the "TRIGGER" activated latach. This is accomplished by setting the RUN/$\overline{\text{HOLD}}$ pin low and thus stopping the Si7135 cycle until the reading is complete.

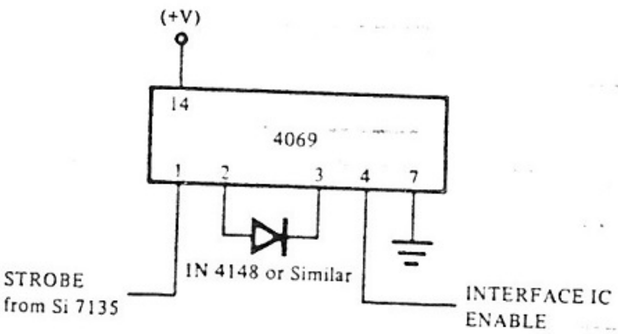

Figure 2
Optional Condition Circuit

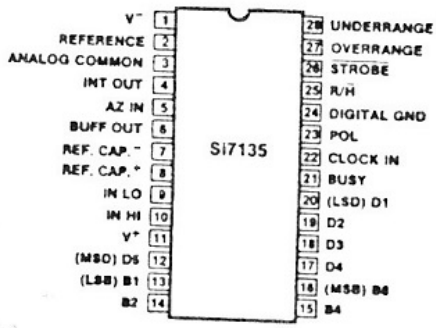

Figure 3
Si7135 Pin Out

Si7135/INTERFACE IC HANDSHAKING

Data is latched into the interface IC from the Si7135 by means of the four BCD data lines (Figure 4). They are routed to the proper character latch by the digit strobe pins. The polarity and most significant digit are simultaneously latched with Digit Strobe One. The $\overline{\text{STROBE}}$ pin, which should not be confused with the five digit strobe pins, goes low five times after each voltage measurement in tandem with the sequencing five digit strobes. Thus, the latching of Si7135 data into the interface IC occurs only once during each measurement cycle as a condition of the

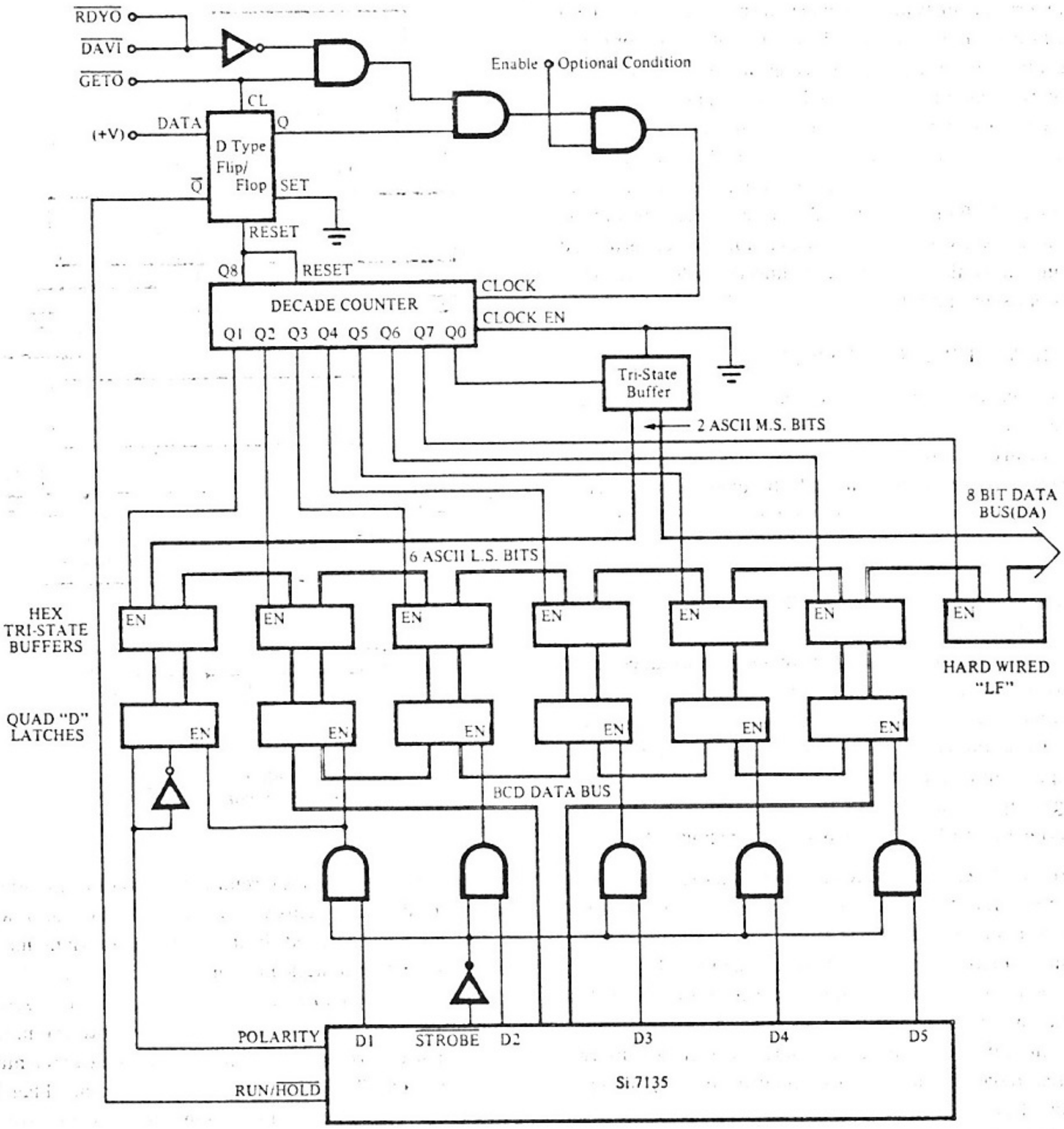

Figure 4
Simplified Circuit of Interface IC

Digit Strobe pins and the STROBE pin. There is one latch for each variable bit of the six variable ASCII characters. Non-variable bits, including the entire "LF" command, are hardwired. These latches and hard wires feed tri-state buffers which are sequentially activated by the counter and consequently present their data to the ASCII output bus (DA) on GPIO.

Autoranging or multiple input select functions can be implemented using similar straightforward programming techniques. The under-range and over-range pins of the Si7135 are connected to the most significant digit buffer. Valid readings on the Si7135 range from −19999 to +19999. The under-range and over-range pins on the Si7135 are tied to the second and third bits of the most significant digit latch. Thus, during under-range, a numerical value slightly greater than or equal to 20,000 will be read, and 40,000 will be read during an over-range condition. These values along with the full register condition of the invalid reading discussed earlier can be checked by software. In the case of over or under-range, a subroutine can be called selecting an appropriately higher or lower scale. The scale called can also indicate the proper coefficient for correct numerical display and decimal placement. Therefore, meter calibration may take place in software if the sensor cannot be adjusted. Under and Overrange as well as other Si7135 functions are optionally used by the designer. The interface IC was designed to allow customizing the interface for a given set of functions and applications. The interface IC is also useful with other A/D converters including the Siliconix "LD" family. Additionally, the great flexibility afforded by the software allows special readings such as dbm, db gain, and radian measure, etc. Indeed, applications of this system seem infinite.

HP-IL/MULTIPLEXER INTERFACE

In the case of input selection, autoranging and function select, etc., the circuit in Figure 5 may be used. Here, eight inputs are used to feed the Si7135. When the multiplexer is receiving instructions, it actually becomes a listener. A relatively simple circuit is required for the interface between the SD5002s and the HP-IL; furthermore, this SD5002 circuit may be used as a stand-alone circuit for a wide range of analog switching functions. SD5002s can be configured into superior video, audio, or RF switching circuits featuring excellent cross-talk and distortion performance (Ref. 2 & 3). Additionally, Siliconix offers a wide range of analog switches and multiplexers to suit any application. Power control is possible with up to 650 volt power FETs and simple standard control circuits. Thus, Siliconix can be a single supplier of specialized components from the HP-IL interface IC to HP-IL controlled high voltage FETs!

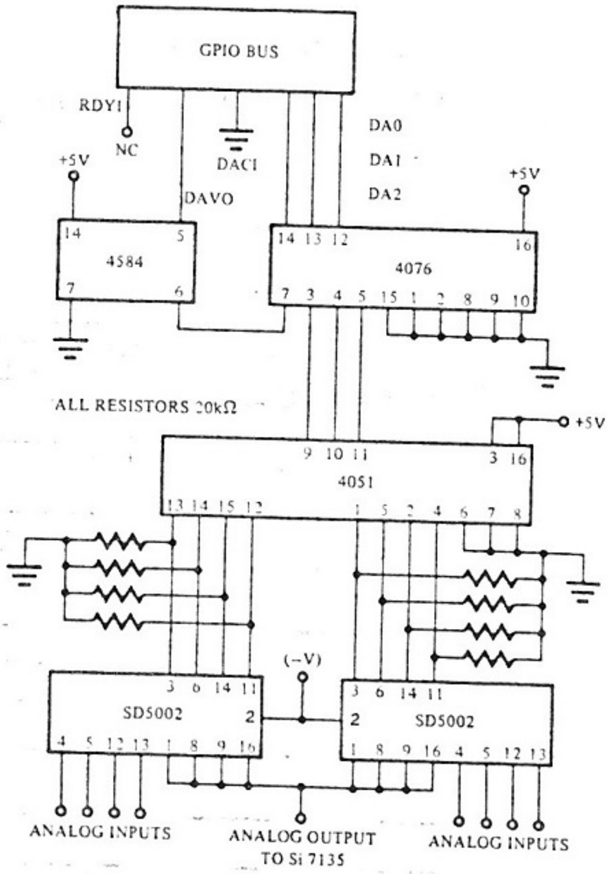

Figure 5
Multiplexer Schematic Diagram

Three 4000 series CMOS ICs are required to interface data from HP-IL to the switch control gates. A separate Si7661 is shown on the multiplexer circuit in case the multiplexer is built independently of the DVM. (Figure 1) If it is built independently, a higher supply voltage can be used. This will allow higher analog voltages to be switched. Siliconix also manufactures the SD210 series which are discrete switch devices; these devices may be used if superior channel isolation is required and/or higher signal voltages must be switched.

HP-IL/multiplexer handshaking is very straightforward. The $\overline{\text{DAVO}}$ pin is used to enable a CMOS latch which stores the last three bits of the transmitted ASCII character. The $\overline{\text{RDYI}}$ pin is not used while the $\overline{\text{DACI}}$ pin is tied to ground. This is the simplest handshake scheme possible with HP-IL.

In the multiplexer, the three least significant bits of the ASCII character taken from the DA bus are used to select one of the eight analog inputs. The "OUTA" command in HP-41 software sends the contents of the Alpha Register to the IL device. The very simple hardware interface requires some special compensation in software. The most important constraint with this circuit is to send only one ASCII character at a time. This will prevent "glitches" and false data from being latched. In its normal operations mode, the HP-41 will automatically send an "End of Data" ASCII character at the end of an alpha string. The last ASCII character sent is the one which is latched into the multiplexer. For this reason, the "End of Data" character must be restrained. This is accomplished by setting Flag 17 "SF17" in the software. A more complex problem involves mathematical manipulations of numbers specifying the multiplexer channel. Such manipulations must take place with digital information-not alpha characters. Since HP-IL can only send data from the Alpha Register, these digital characters must be sent to the Alpha Register for transmission to the multiplexer. A problem arises because a decimal point "rides along" with the number to the Alpha Register. The decimal point is consequently read by the IL interface and sent as a ASCII character to the multiplexer causing a "glitch" or an invalid latch. This problem can be solved by clearing Flag 29 "CF29" and not displaying fraction data "FIXO". With these two additional simple commands, the desired numeric ASCII character will be latched into the multiplexer.

SOFTWARE EXAMPLE

Table 2 shows a simple program which will sequence the eight input multiplexer, display the input channel number, read in the voltage, display the voltage, and loop back. It is included to provide a sample program to get the system working and illustrate how the necessary commands can be arranged. The power of the HP-IL system may be appreciated when one sees only 29 lines of programming! The user will in most instances modify or rewrite programs to meet individual needs.

Details of HP software are contained in the literature provided with the applicable HP devices. The HP 82166C Interface Kit includes a very comprehensive system description of HP-IL contained in multiple volumes. One word of caution to the hardware designer: there are numerous errors and misleading diagrams in the HP booklet entitled "HP 82166A HP-IL Converter Technical Manual" (Nov. 81). The corrections to these errors are in a follow-up booklet "HP-IL/GPIO Interface HP-IL Converter Manual Supplement".

In conclusion, Siliconix now offers the necessary integrated circuits to easily facilitate HP-IL interface to a low cost DVM design. This solution reduces the problem of such an interface to an easy lay-out task.

Table 1

```
01 LBL DVM1
02 LBL 01
03 TRIGGER
04 IND
05 VIEW X
06 GTO 01
07 END
```

Table 2

```
01 LBL DVM1      16 -
02 0             17 X=0?
03 STO 01        18 GTO 03
04 LBL 02        19 RCL 01
05 VIEW X        20 1
06 TRIGGER       21 +
07 IND           22 LBL 03
08 .0001         23 STO 01
09 •             24 CLA
10 FIX 4         25 ARCL 01
11 VIEW X        26 SF 17
12 FIX 0         27 OUTA
13 CF 29         28 GTO 02
14 RCL 01        29 END
15 7
```

REFERENCES:

1. *Electronic Design, Parzybok, Hanson,* Dec. 24, 1981.
2. Siliconix Application Note: *"A High Performance Video Switch", Zavrel.*
3. Siliconix Application Note: *"A High Quality Audio Crosspoint Switch", Zavrel.*

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