PIL-IO board notes

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1. General Description

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1. General Description:

The PIL-IO board provides 4 digital input/output lines and a serial link to the HP-IL loop. It can be driven by any HP-IL controller such as the HP-41C or the HP-71B. The PIL-IO board is intended to be used by electronic hobbysts.

The PIL-IO board provides 2 HP-IL device functions at the same time:

- a mini HP-IL/GPIO interface with 4 I/O lines,

- a mini HP-IL/serial interface with logic level Rx and Tx lines.

The 4 I/O lines can be used either as inputs or outputs in any combination. The serial Tx and Rx lines can be used to interface with an other microcontroller using an asynchronous serial communication link (UART). All the I/O and Rx/Tx lines are 5V logic (TTL/CMOS compatible logic)

The power supply is not included. A 5V supply has to be provided by the user to the board.

The PIL-IO will work with any HP-IL controler such as the HP-41C, HP-71B or HP-75C.

With the HP-41C, OUTA is used to set the 4 I/O lines, by sending a hexa-coded character that is the binay value corresponding to lines 0-3:

For instance "0" OUTA clears all lines 0 to 3,

"2" OUTA sets line 1, and clears lines 0, 2, 3.

INSTAT reads the status of the I/O lines, the result is in flags 0 to 3 and decimal value in X.

With the HP71, the equivalent commands are: OUTPUT :1,"0" clears all lines 0 to 3, OUTPUT :1,"2" sets line 1, and clears lines 0, 2, 3. X=SPOLL(1) read the status of the I/O lines, the result is in the variable X

This document gives the necessary information to connect the board and use it with a HP-41C or HP-71B and their respective HP-IL module.

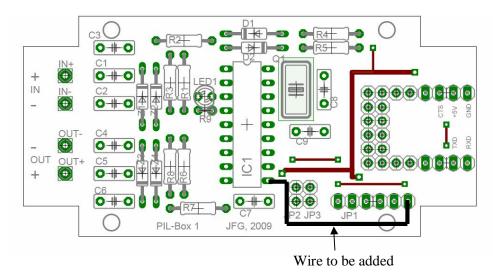
2. PIL-IO Board Description and Setup

PIL-IO board kit



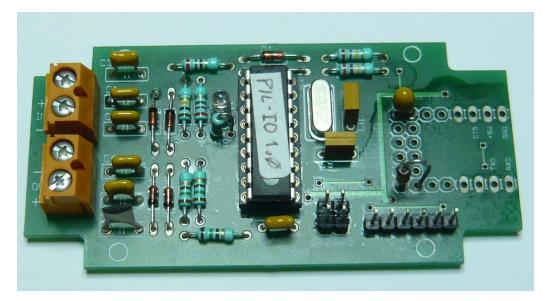
- 1 PCB
- 1 programmed microcontroller PIC 16F628A
- 1 component set:
 - o R1..R9
 - o C1..C9
 - o D1, D2
 - o Z1, Z2, Z3, Z4
 - o LED
 - o Crystal 20 MHz
 - o Zener diode BZX85 5.6V
 - o capacitor 4.7uF 25V
 - o 18 pts socket for the uC
 - o connectors for HP-IL cable (2) with wire terminals (4)
 - o I/O connectors: JP1 6pts , JP2/JP3 2 pts

PCB layout:



Bill of Material:

| R1, R2: | 220 Ohms | | | |
|---------------|---|--|--|--|
| R3: | 10 kOhms | | | |
| R4, R5: | 22 kOhms | | | |
| R6, R7, R8: | 150 Ohms | | | |
| R9: | 470 Ohms – vertical mounting, used only if LED1 is mounted | | | |
| C1, C2, C4, C | C5: 22 nF – 100V rating | | | |
| C3, C7: | 100 nF | | | |
| C6: | 120 pF | | | |
| C8, C9: | 22 pF | | | |
| D1, D2: | 1N4148 | | | |
| Z1, Z2, Z3, Z | 4: BZX55-5.1V | | | |
| LED1: | 3mm LED, red (optional) – cathode (shortest lead) towards IC1 | | | |
| Q1: | 20 MHz crystal | | | |
| IC1: | Microchip 16F628A (on socket) | | | |
| | | | | |

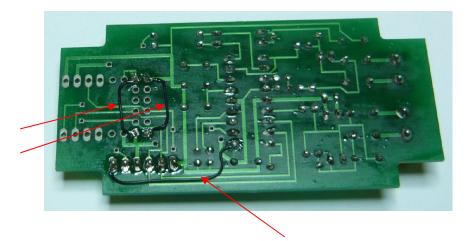


Additional wiring for the PIL-IO board:

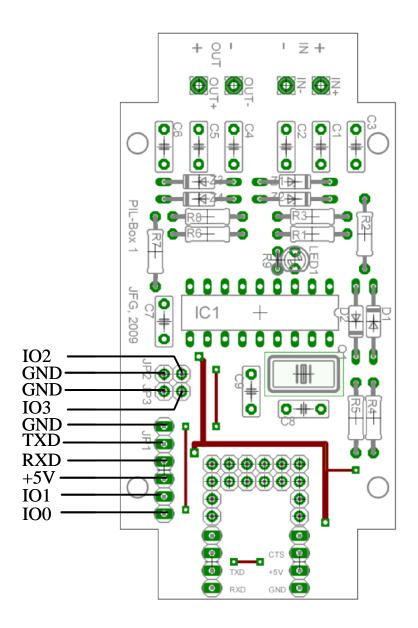
A wire is need between IC1, pin 10 and JP1, pin 6 (see above).

It is recommended to mount a 4.7 to 10uF capacitor (16V min, prefered tantalium for small size) and a 5.6V Zener diode (BZX85 5.6V) on the supply lines on the board, for proper decoupling and protection against incorrect voltage or polarity. Below is the suggested wiring for these 2 components:





PIL-IO supply and I/O connectors:



HP-IL cable wiring:

The IN and OUT cables must be wired like this:



See the original PIL-Box setup document for more details.

PIL-IO board basic test:

Apply a 5V supply to the PIL-IO board. The LED should blink 3 times. If yes, the uC is working correctly.

Connect a HP-41C or HP71B to the PIL-IO:

- HP-41C:
 - do "PILPIO1" FINDID.

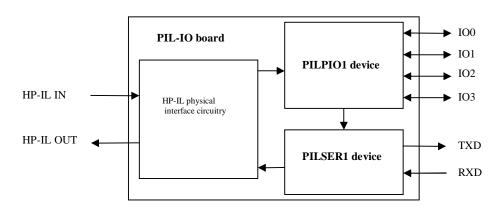
If the result is 1, then the PIL-IO board is working correctly and the HP-IL cables are correctly wired.

 HP-71B: do RESTORE IO, then DEVADDR("PILPIO1")
 If the result is 1, then the PIL-IO board is working correctly and the HP-IL cables are correctly wired.

3. PIL-IO Board Usage

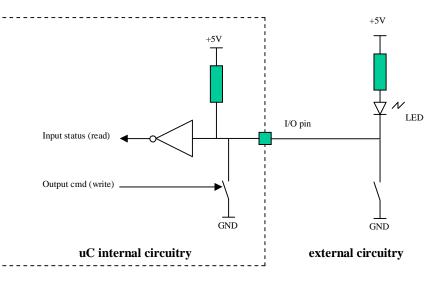
The PIL-IO board provides 2 HP-IL device functions at the same time: - "PILPIO1": a mini HP-IL/GPIO interface with 4 I/O lines,

- "PILSER1": a mini HP-IL/serial interface with logic level Rx and Tx lines.



PILPIO1 device:

The 4 I/O lines IO0 to IO3 are used for both input and output. No special configuration is needed. The I/O structure is like this:



Writing a '1' to the output drives the I/O low (closed to ground). An external load connected between the I/O pin and the +5V (such as a LED as indicated) is activated.

Writing a '0' to the output drives the I/O high (pulled up by the internal resistor). The LED is off.

The output drive capability is up to 8.5mA when the I/O is driven low. The internal pullup resistor provides about 200uA.

To use an I/O as an input, write '0' to the output. With no external signal applied on the I/O pin, the status is 0. If the I/O line is driven low (for instance by an external switch as indicated), then the status is 1.

The inputs are TTL compatible.

See the electrical specification of the PIC16F628A uC on next page for more details.

| Sym | Characteristic/Device | Min | Typ† | Max | Unit | Conditions | | |
|-------|---|--------------------------|------|----------|---------|---|--|--|
| VIL | Input Low Voltage | | | | | | | |
| | I/O ports with TTL buffer | Vss | | 0.8 | v | VDD = 4.5V to 5.5V | | |
| | | Vss | | 0.15 VDD | Γ ý | otherwise | | |
| | with Schmitt Trigger input ⁽⁴⁾ | Vss | | 0.2 VDD | v | 222202020 | | |
| | MCLR, RA4/T0CKI,OSC1 (in RC mode) | Vss | 1000 | 0.2 VDD | v | (Note 1) | | |
| | OSC1 (in HS) | Vss | | 0.3 VDD | v | | | |
| | OSC1 (in LP and XT) | VSS | | 0.6 | Ň | | | |
| VIH | Input High Voltage | | | | | | | |
| | I/O ports | | | | | | | |
| | with TTL buffer | 2.0V | | VDD | V. | VDD = 4.5V to 5.5V | | |
| | | .25 VDD + 0.8V | | VDD | V | otherwise | | |
| | with Schmitt Trigger input ⁽⁴⁾ | 0.8 VDD | 3000 | VDD | V | | | |
| | MCLR RA4/TOCKI | 0.8 VDD | 1 | VDD | V | | | |
| | OSC1 (XT and LP) | 1.3 | 1000 | VDD | V | | | |
| | OSC1 (in RC mode) | 0.9 VDD | _ | VDD | V | (Note1) | | |
| | OSC1 (in HS mode) | 0.7 VDD | | VDD | V | - 22 - 2707) | | |
| IPURB | PORTB weak pull-up current | 50 | 200 | 400 | μΑ | VDD = 5.0V, VPIN = VSS | | |
| İL | nput Leakage Current ^{(2), (3)} | | | | | | | |
| | I/O ports (Except PORTA) | 2 | _ | ±1.0 | μA | VSS ≤ VPIN ≤ VDD, pin at high-impedance | | |
| | PORTA ⁽⁴⁾ | 2000 20 00 | | ±0.5 | щA | VSS ≤ VPIN ≤ VDD, pin at high-impedance | | |
| | RA4/T0CKI | 2000 | | ±1.0 | μA | VSS ≤ VPIN ≤ VDD | | |
| | OSC1, MCLR | _ | | ±5.0 | μA | VSS ≤ VPIN ≤ VDD, XT, HS and LP | | |
| | | | | 2012200 | 2334623 | oscillator configuration | | |
| VOL | Output Low Voltage | | | | | | | |
| | | 3 9 | - | 0.6 | V | IOL = 8.5 mA, VDD = 4.5 V, -40° to +85°C | | |
| | I/O ports ⁽⁴⁾ | 1922 | - | 0.6 | V | IOL = 7.0 mA, VDD = 4.5 V, +85° to +125°C | | |
| VOH | Output High Voltage ⁽³⁾ | | | | | | | |
| | I/O ports (Except RA4 ⁽⁴⁾) | VDD - 0.7 VDD - 0.7 | _ | — | v v | IOH = -3.0 mA, VDD = 4.5 V, -40° to +85° IOH = -2.5 mA, VDD = 4.5 V, +85° to +125°C | | |

PIC16F628A I/O specification.

| IO0 | I01 | IO2 | IO3 | Decimal | Hexa char. |
|------------|------------|-----|------------|---------|------------|
| 0 | 0 | 0 | 0 | 0 | "0" |
| 1 | 0 | 0 | 0 | 1 | "1" |
| 0 | 1 | 0 | 0 | 2 | "2" |
| 1 | 1 | 0 | 0 | 3 | "3" |
| 0 | 0 | 1 | 0 | 4 | "4" |
| 1 | 0 | 1 | 0 | 5 | "5" |
| 0 | 1 | 1 | 0 | 6 | "6" |
| 1 | 1 | 1 | 0 | 7 | "7" |
| 0 | 0 | 0 | 1 | 8 | "8" |
| 1 | 0 | 0 | 1 | 9 | "9" |
| 0 | 1 | 0 | 1 | 10 | "A" |
| 1 | 1 | 0 | 1 | 11 | "B" |
| 0 | 0 | 1 | 1 | 12 | "C" |
| 1 | 0 | 1 | 1 | 13 | "D" |
| 0 | 1 | 1 | 1 | 14 | "Е" |
| 1 | 1 | 1 | 1 | 15 | "F" |

I/O state, decimal values read for input, hexa character to be written for output:

Programming examples with the HP-41C:

LBL "IOEX1" "PILPIO1" FINDID SELECT 10 LBL 01 "1" OUTA "2" OUTA "4" OUTA "8" OUTA "8" OUTA DSE X GTO 01 This example successively drives the 4 lines IO0 to IO3 low 10 times.

```
LBL "IOEX2"

"PILPIO1" FINDID SELECT

"0" OUTA

LBL 01

INSTAT

VIEW X

GTO 01

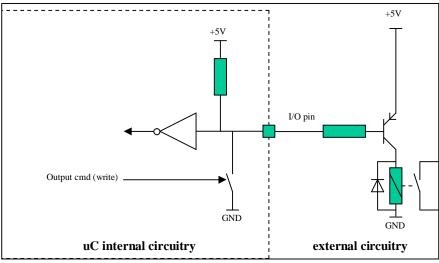
This example continusly reads the I/O status and displays it in flags 0-3 and as a decimal

value in X.
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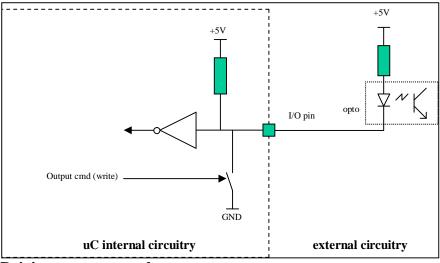
With the Extended I/O module HP82183A:

CLRDEV or CLRLOOP: drives all the I/O line to 0 (open). ID: returns "PILPIO1A". The 'A' character indicates the firmware revision. AID: returns 64. 64 FINDAID: finds the PILPIO1 address.

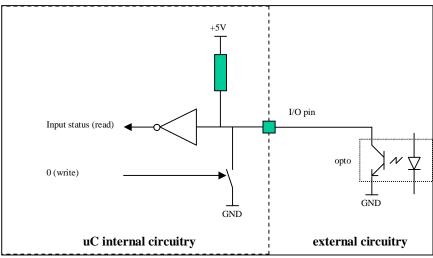
Application examples:



Driving a relay with an external transistor



Driving an opto-coupler output



Reading an opto-coupler input

PILSER1 device:

The TXD and RXD serial lines are logic +5V CMOS signals, coming from the USART of the PIC16F628A uC. They are NOT at RS232 level.

The primary function of the serial lines is to interface with an external microcontroller to extend the functionalities of the PIL-IO.

The USART is programmed as: 9600 bps, 8 bits, 1 start, 1 stop, no parity.

No hardware or software handshake is provided. There is a 64 bytes input buffer.

A status byte is available. It can be read by the HP-IL controller to get the status of the serial communications (HP-41C: INSTAT function, HP-71B: SPOLL function).

| | Status Syte Iollian | | |
|-----|---------------------|--|--|
| Bit | Value | Description | |
| 0 | 1 | Data available in the receive buffer. Cleared when buffer is empty | |
| 1 | 2 | Line-feed (10 decimal) received. Cleared after reading the status byte | |
| 2 | 4 | (unused) | |
| 3 | 8 | Buffer overflow. Cleared after reading the status byte | |
| 4 | 16 | Framing error. Cleared after reading the status byte | |

Status byte format:

Bit 0 can be used to check if there is some data in the received buffer.

Bit 1 can be used to check if a complete line ending with LF has been received

Bits 3 and 4 are for error checking. Bit 3 is set if more than 64 bytes are received. Bit 4 is set if a character is not correctly received (for instance no stop bit detected), usually meaning that the transmission rate is not consistent between transmitter and receiver.

Programming example with the HP-41C:

LBL "IOEX3" "PILSER1" FINDID SELECT INSTAT INA "ABCDEF" OUTA INSTAT INA

This example reads the status byte and input buffer to clear any previous state, sends the string "ABCDEF", then reads the status byte and the input buffer.

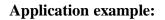
If the RXD and TXD lines are connected together (local loopback), then the flags 0 and 1 will be set and the ALPHA register will hold "ABCDEF".

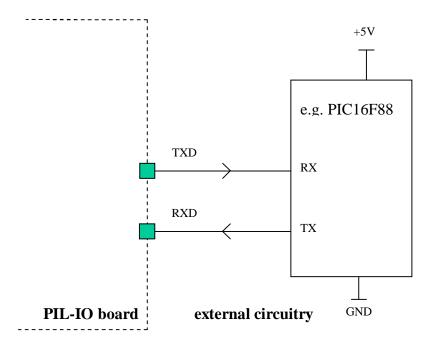
With the Extended I/O module HP82183A:

CLRDEV or CLRLOOP: clears the input buffer and status byte.ID: returns "PILSER1A". The 'A' character indicates the firmware revision.AID: returns 66.66 FINDAID: finds the PILSER1 address.The INAN, OUTAN, etc variants can be used for advanced communication management.

Note:

If the serial lines are not used, do not leave the RXD line unconnected, for instance put a jumper between RXD and TXD on the connector JP1.





Connection between the PIL-IO serial lines and an external circuitry.